Chipwell Tech Corporation

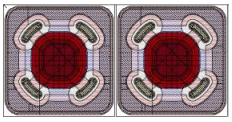
Wafer Specification Sheet

CE13L05P0S2 2-Channel Ultra Low Capacitance ESD Diode Array

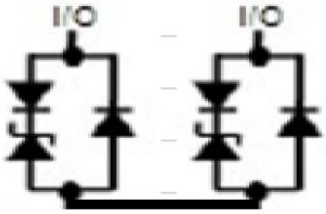
Wafer Information

Item	Description
Wafer Size	6 inch (150mm)
Wafer Thickness	150um ± 10um
Die Size (with scribe lane)	334um x 186um
Bond Pad Opening	71um x 71um
Scribe Lane Width	40um
Gross Die Per Wafer	250,000
Top Metal (for wire bond)	4μm AlSiCu
Backside Metal (for die bond)	TiNiAgSn 1/3/5/14 KA

Die Appearance



Circuit Diagram



- Complies with IEC 61000-4-2 standards:
  Contact discharge: ±20kV

Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20μs)	Ppk	72	W
Peak Pulse Current (8/20μs)	IPP	4	A
Operating Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	Tstg	−55 to +150	°C

Electrical Characteristics (T_A=25°C unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	VRWM			5	V	
Breakdown Voltage	VBR	6.0			V	IT = 1mA
Reverse Leakage Current	I_R			100	nA	VRWM = 5V
Forward voltage	VF			1.2	V	IF=15mA
Clamping Voltage	VC		10		V	IPP = 1A (8 x 20μs pulse)
Clamping Voltage	VC		18		V	IPP = 4A (8 x 20μs pulse)
Junction Capacitance	C_J		0.25	0.35	pF	VR = 0V, f = 1MHz

Note: Electrical parameters are only for die, performance may alter after assembly.