

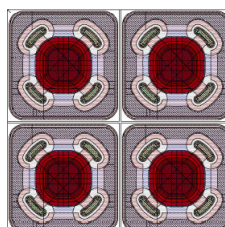
### **CE13L03P3G4 4-Channel Ultra Low Capacitance ESD Diode Array**

#### Wafer Information

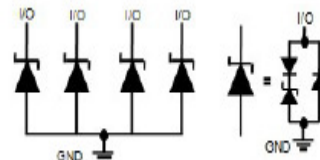
Item	Description
Wafer Size	6 inch (150mm)
Wafer Thickness	150um ± 10um
Die Size (with scribe lane)	334um x 334um
Bond Pad Opening	71um x 71um
Scribe Lane Width	40um
Gross Die Per Wafer	143,000
Top Metal (for wire bond)	4μm AlSiCu
Backside Metal (for die bond)	Ag

- Complies with IEC 61000-4-2 standards:  
Contact discharge: ±20kV

#### Die Appearance



#### Circuit Diagram



#### Absolute Maximum Ratings (T<sub>A</sub>=25 °C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20μs)	P <sub>pk</sub>	56	W
Peak Pulse Current (8/20μs)	I <sub>PP</sub>	4	A
Operating Temperature Range	T <sub>J</sub>	-55 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C

#### Electrical Characteristics (T<sub>A</sub>=25 °C unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	VRWM			3.3	V	
Breakdown Voltage	VBR	4.2			V	I <sub>T</sub> = 1mA
Reverse Leakage Current	I <sub>R</sub>			100	nA	VRWM = 3.3V
Forward voltage	V <sub>F</sub>			1.2	V	I <sub>F</sub> =15mA
Clamping Voltage	V <sub>C</sub>			10	V	I <sub>PP</sub> = 1A (8 x 20μs pulse)
Clamping Voltage	V <sub>C</sub>			14	V	I <sub>PP</sub> = 4A (8 x 20μs pulse)
Junction Capacitance	C <sub>J</sub>		0.45	0.60	pF	VR = 0V, f = 1MHz, I/O to GND
Junction Capacitance	C <sub>J</sub>		0.22	0.30	pF	VR = 0V, f = 1MHz, IO to IO

**Note:** Electrical parameters are only for die, performance may alter after assembly.