Chipwell Tech Corporation

Wafer Specification Sheet

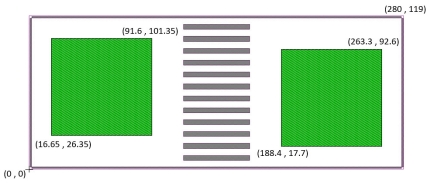
CE13S01P5N2 Preliminary

Ultra Low Capacitance ESD Protection Device

Wafer Information

Item	Description
Wafer Size	6 inch (150mm)
Wafer Thickness	690 ± 25 um
Die Size (with scribe line)	320um x 159um
Bond Pad Opening	75um x 75um
Scribe Lane Width	40um
Gross Die Per Wafer	290,000
Top Metal (for wire bond)	2.5µm AlSiCu
Backside Metal (for die bond)	N/A

Die Appearance



Circuit Diagram

- Complies with IEC 61000-4-2 standards:
  Contact discharge: ±12kV

Absolute Maximum Ratings (T_A=25℃ unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20µs)	Ppk	12	W
Peak Pulse Current (8/20µs)	IPP	4	A
Operating Temperature Range	T_J	–55 to +125	℃
Storage Temperature Range	Tstg	–55 to +150	℃

Electrical Characteristics (T_A=25℃ unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	VRWM			1.5	V	
Breakdown Voltage	VBR	4.0	6.0		V	IT = 100uA
Reverse Leakage Current	I_R			100	nA	VRWM = 1.5V
Clamping Voltage	VC		1.75		V	IPP = 1A (8 x 20µs pulse)
Clamping Voltage	VC		2.9		V	IPP = 4A (8 x 20µs pulse)
Junction Capacitance	C_J		0.2		pF	VR = 0V, f = 1MHz
ESD Dynamic Turn on Resistance	R_{dyn}		0.25		Ω	IEC 61000-4-2 0~+8kV, Contact mode, T=25℃

Note: Electrical parameters are only for die, performance may alter after assembly.

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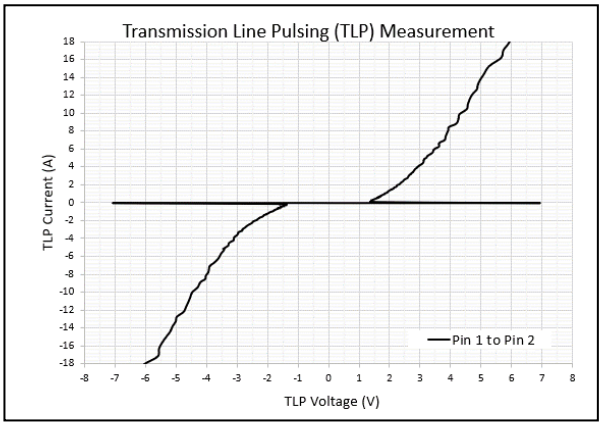
TLP (TA=25℃ unless otherwise specified)



Typical Variation of CIN vs. VIN)