

### CE13S03P3N2

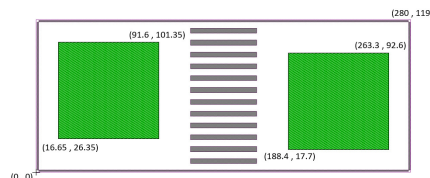
**Preliminary**

### Ultra Low Capacitance ESD Protection Device

#### Wafer Information

Item	Description
Wafer Size	6 inch (150mm)
Wafer Thickness	690 ± 25 μm
Die Size (with scribe line)	320μm x 159μm
Bond Pad Opening	75μm x 75μm
Scribe Lane Width	40μm
Gross Die Per Wafer	290,000
Top Metal (for wire bond)	2.5μm AlSiCu
Backside Metal (for die bond)	N/A

#### Die Appearance



#### Circuit Diagram



- Complies with IEC 61000-4-2 standards:  
Contact discharge: ±12kV

#### Absolute Maximum Ratings (T<sub>A</sub>=25°C unless otherwise specified)

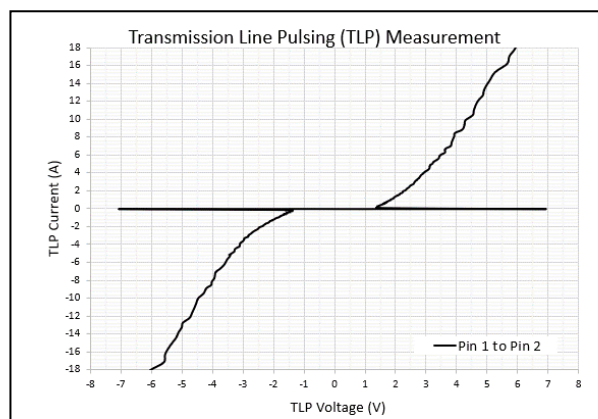
Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20μs)	P <sub>pk</sub>	20	W
Peak Pulse Current (8/20μs)	I <sub>PP</sub>	4	A
Operating Temperature Range	T <sub>J</sub>	-55 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C

#### Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	VRWM			3.3	V	
Breakdown Voltage	VBR	4.5	6.5		V	I <sub>T</sub> = 100uA
Reverse Leakage Current	I <sub>R</sub>			100	nA	VRWM = 3.3V
Clamping Voltage	VC		1.75		V	I <sub>PP</sub> = 1A (8/20μs pulse, T=25°C)
Clamping Voltage	VC		2.9		V	I <sub>PP</sub> = 4A (8/20μs pulse, T=25°C)
Junction Capacitance	C <sub>J</sub>		0.25		pF	VR = 0V, f = 1MHz
ESD Dynamic Turn on Resistance	R <sub>dyn</sub>		0.25		Ω	IEC 61000-4-2 0~+8kV, Contact mode, T=25°C

**Note:** Electrical parameters are only for die, performance may alter after assembly.

### TLP (TA=25°C unless otherwise specified)



### Typical Variation of CIN vs. VIN

