Chipwell Tech Corporation

Wafer Specification Sheet

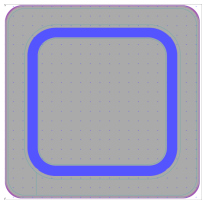
CE10L05P0S1 1-channel ultra low capacitance ESD diode

Preliminary

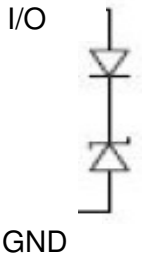
Wafer Information

Item	Description
Wafer Size	6 inch (150mm)
Wafer Thickness	150um ± 10um
Die Size (with scribe lane)	246um x 246um
Bond Pad Opening	121um x 121um
Scribe Lane Width	40um
Gross Die Per Wafer	258,400
Top Metal (for wire bond)	AlSiCu 4μm
Backside Metal (for die bond)	TiNiAgSn 1/3/5/14KÅ

Die Appearance



Circuit Diagram



- Complies with IEC 61000-4-2 standards:
  Contact discharge: ±30kV

Absolute Maximum Ratings (T_A=25℃ unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20μs)	Ppk	230	W
Peak Pulse Current (8/20μs)	IPP	14	A
Operating Temperature Range	T_J	–55 to +125	℃
Storage Temperature Range	Tstg	–55 to +150	℃

Electrical Characteristics (T_A=25℃ unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	VRWM			5	V	
Breakdown Voltage	VBR	6			V	IT = 1mA
Reverse Leakage Current	I_R			100	nA	VRWM = 5V
Clamping Voltage	VC		8.0		V	IPP = 1A (8 x 20μs pulse)
Clamping Voltage	VC			13	V	IPP = 7A (8 x 20μs pulse)
Clamping Voltage	VC			17	V	IPP = 14A (8 x 20μs pulse)
Junction Capacitance (Single Die I/O to GND)	C_J		0.7	0.85	pF	VR = 0V, f = 1MHz

Note: Electrical parameters are only for die, performance may alter after assembly.